

Fig. 1

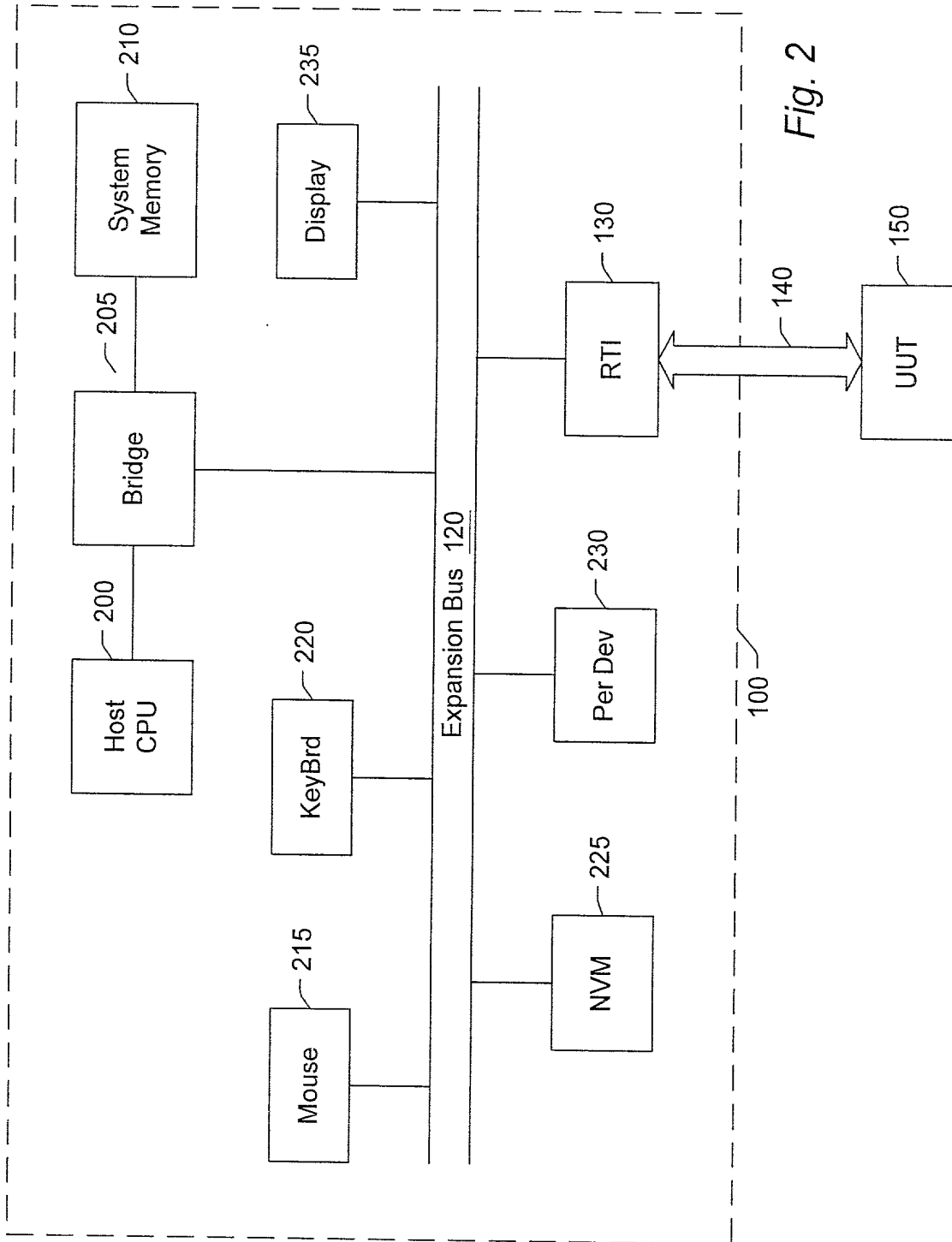


Fig. 2

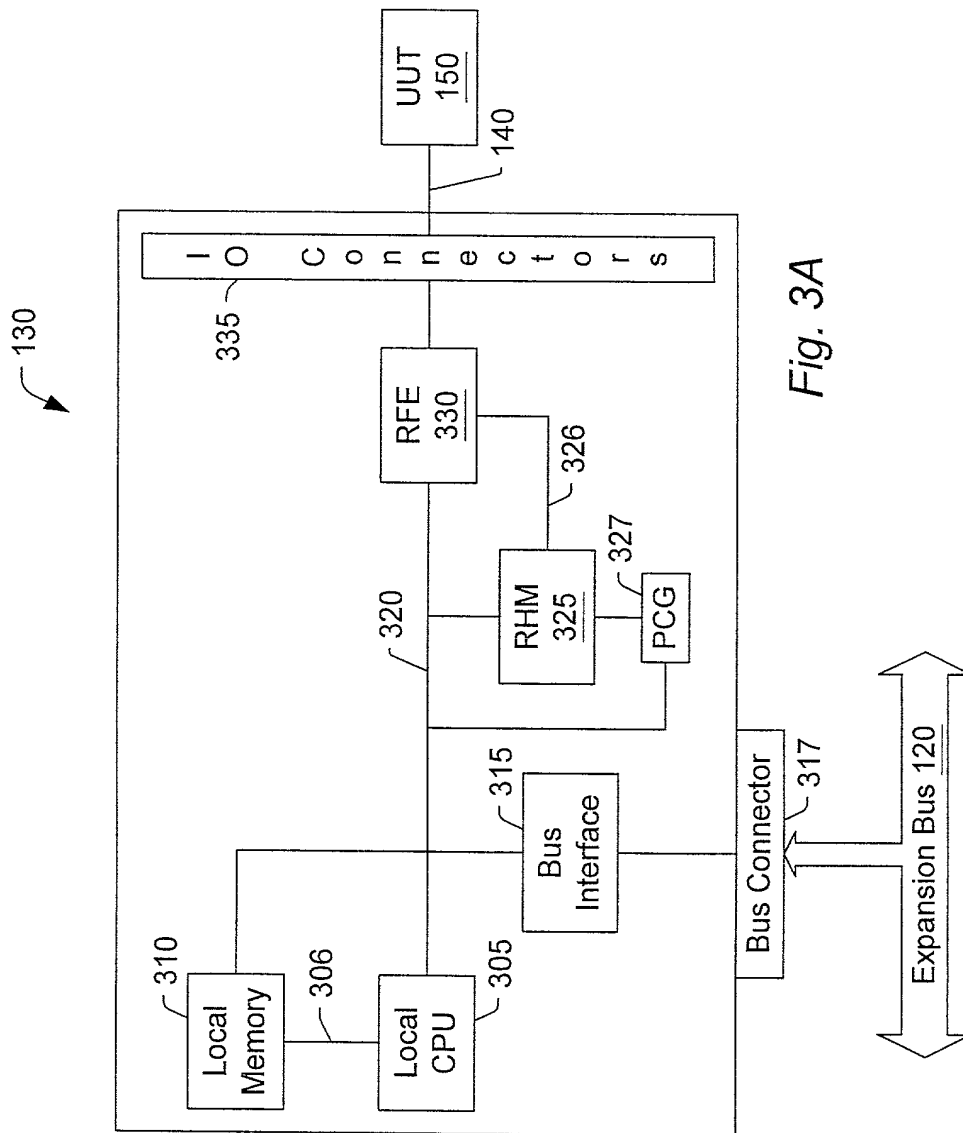


Fig. 3A

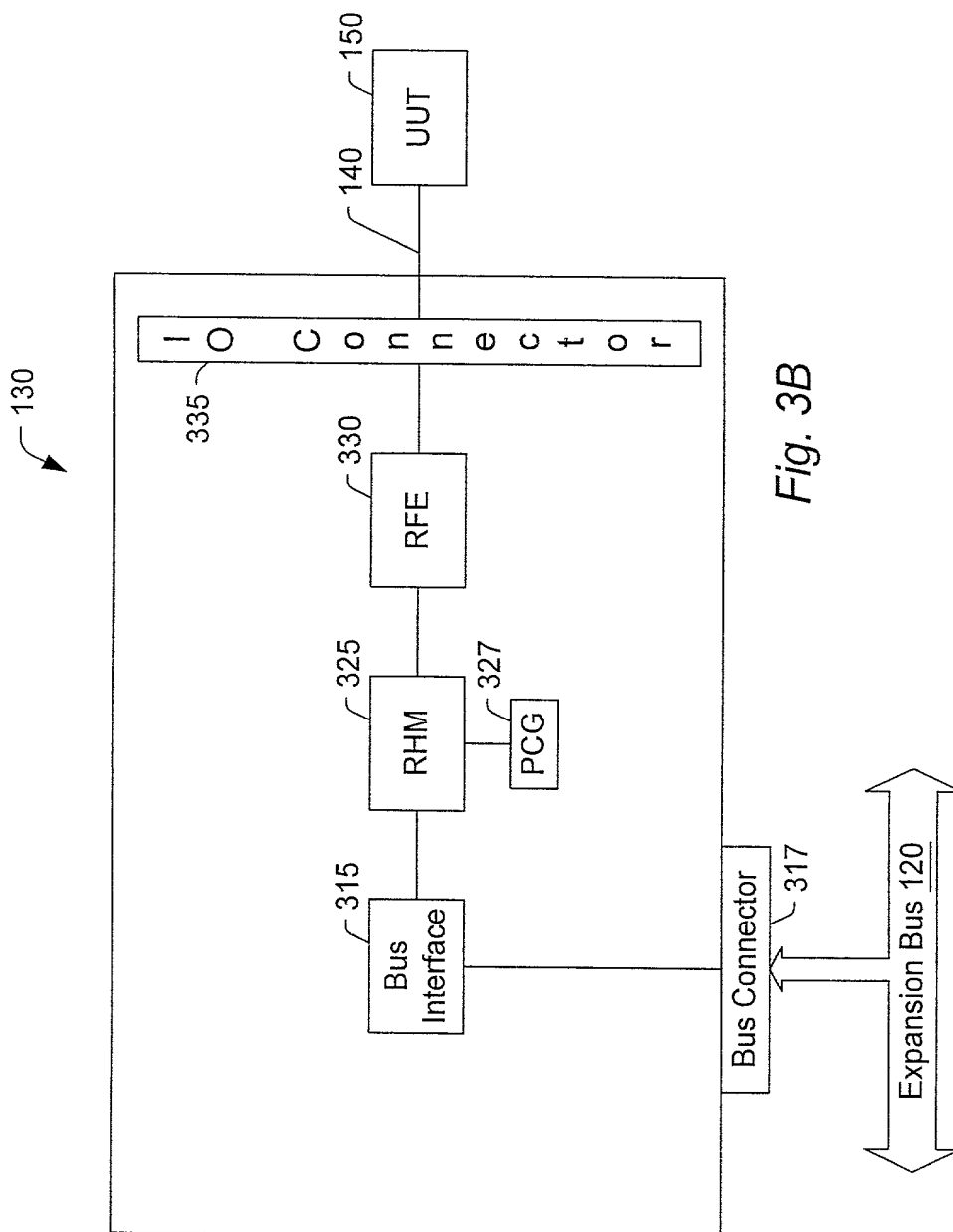


Fig. 3B

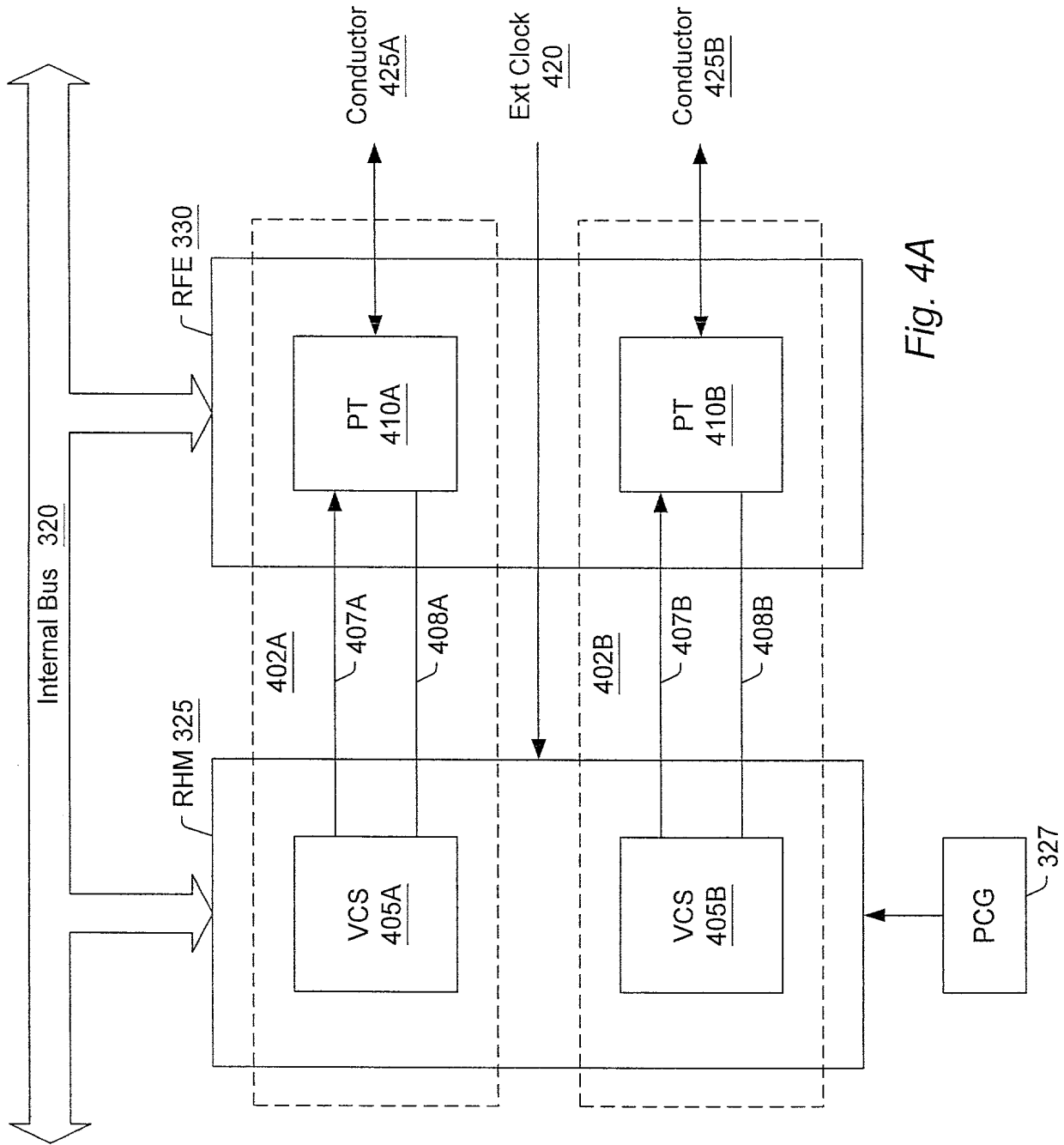


Fig. 4A

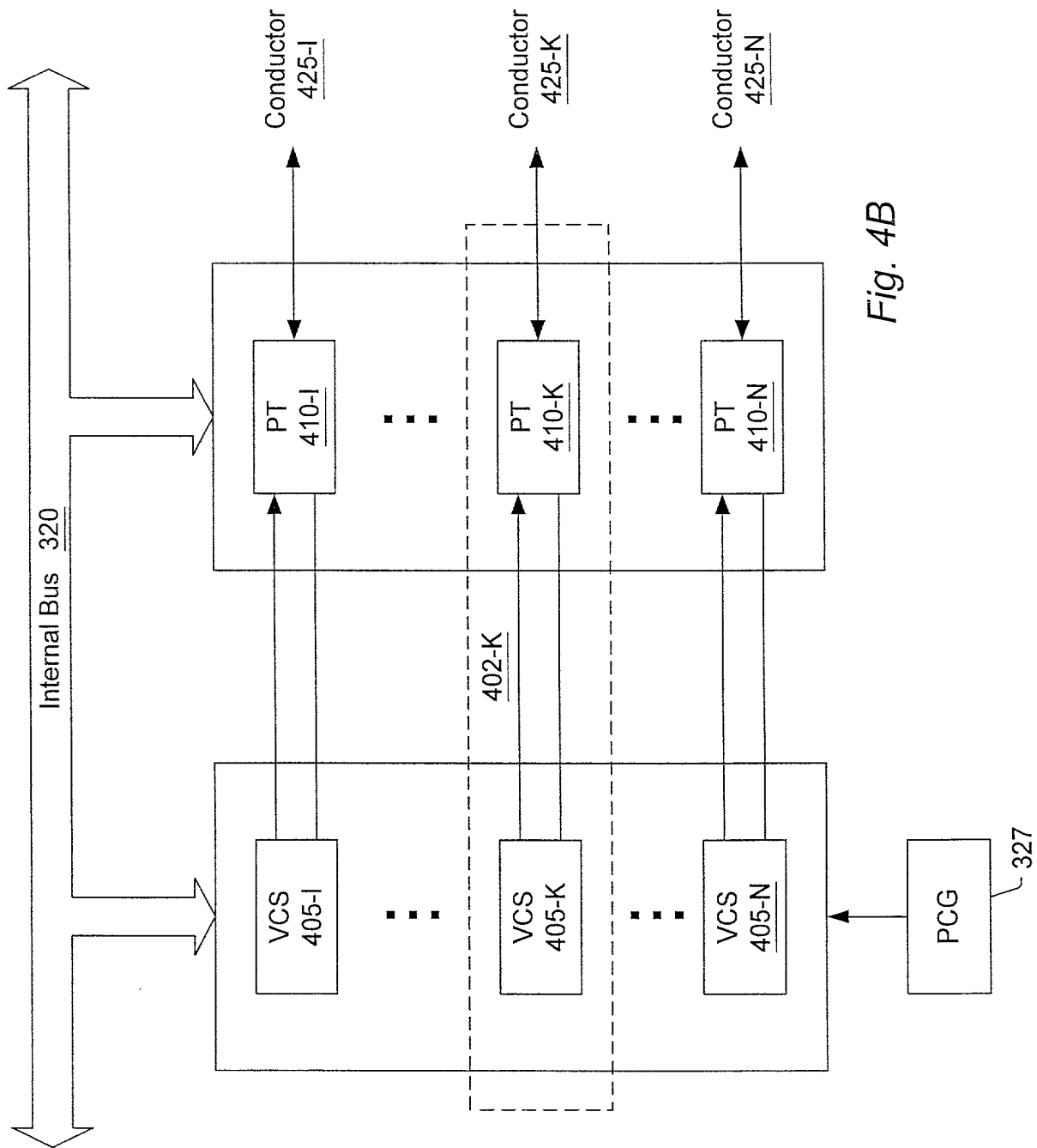
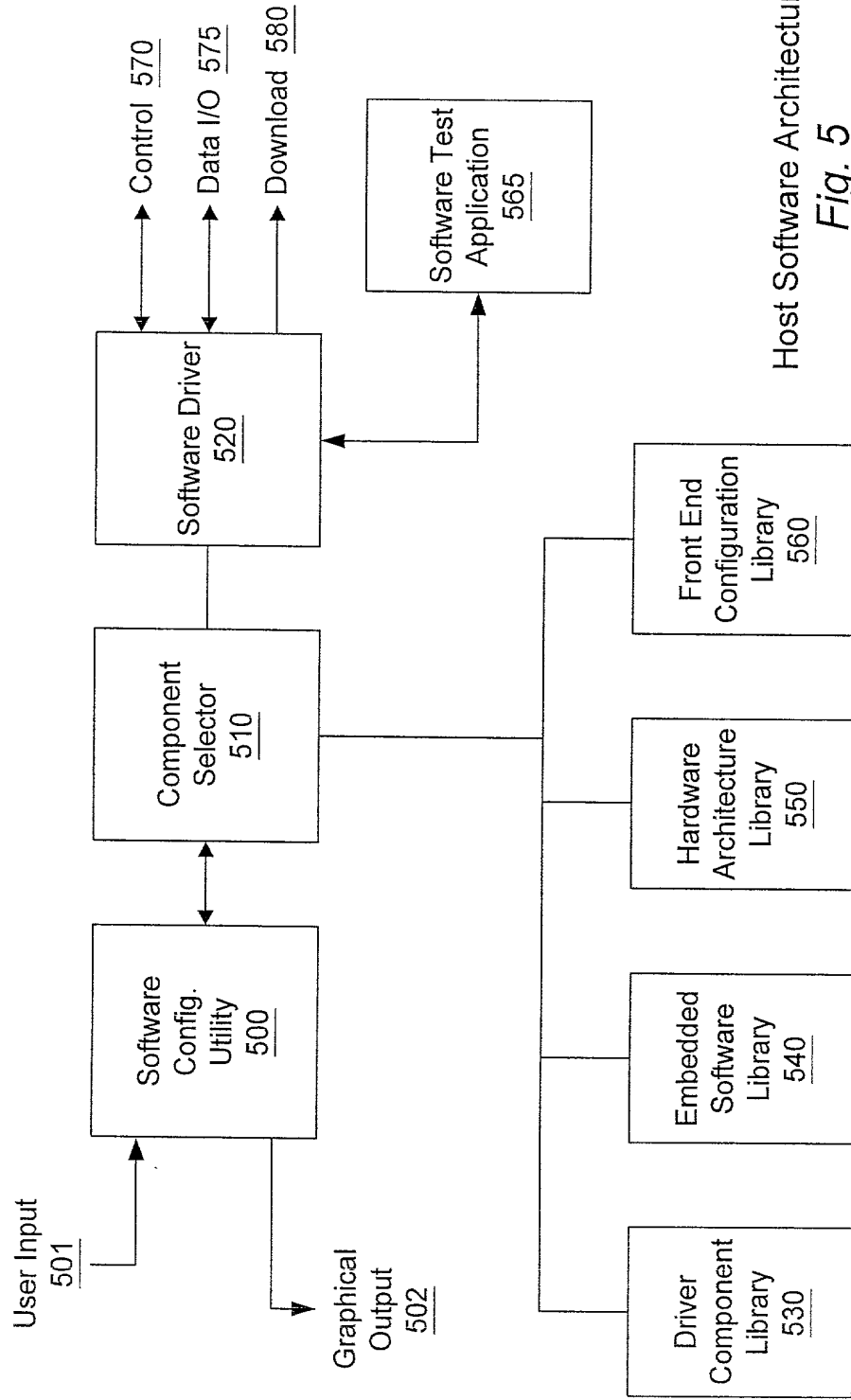


Fig. 4B



Host Software Architecture  
Fig. 5

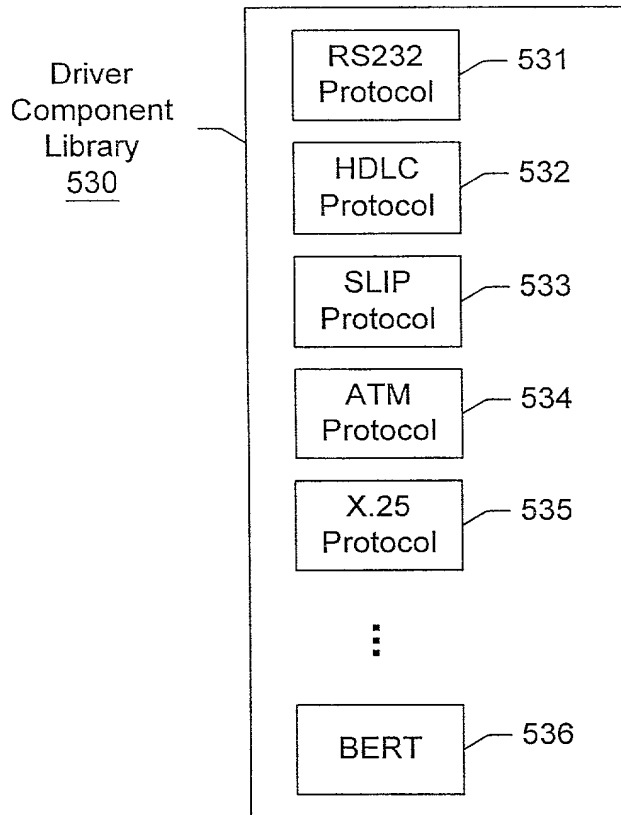
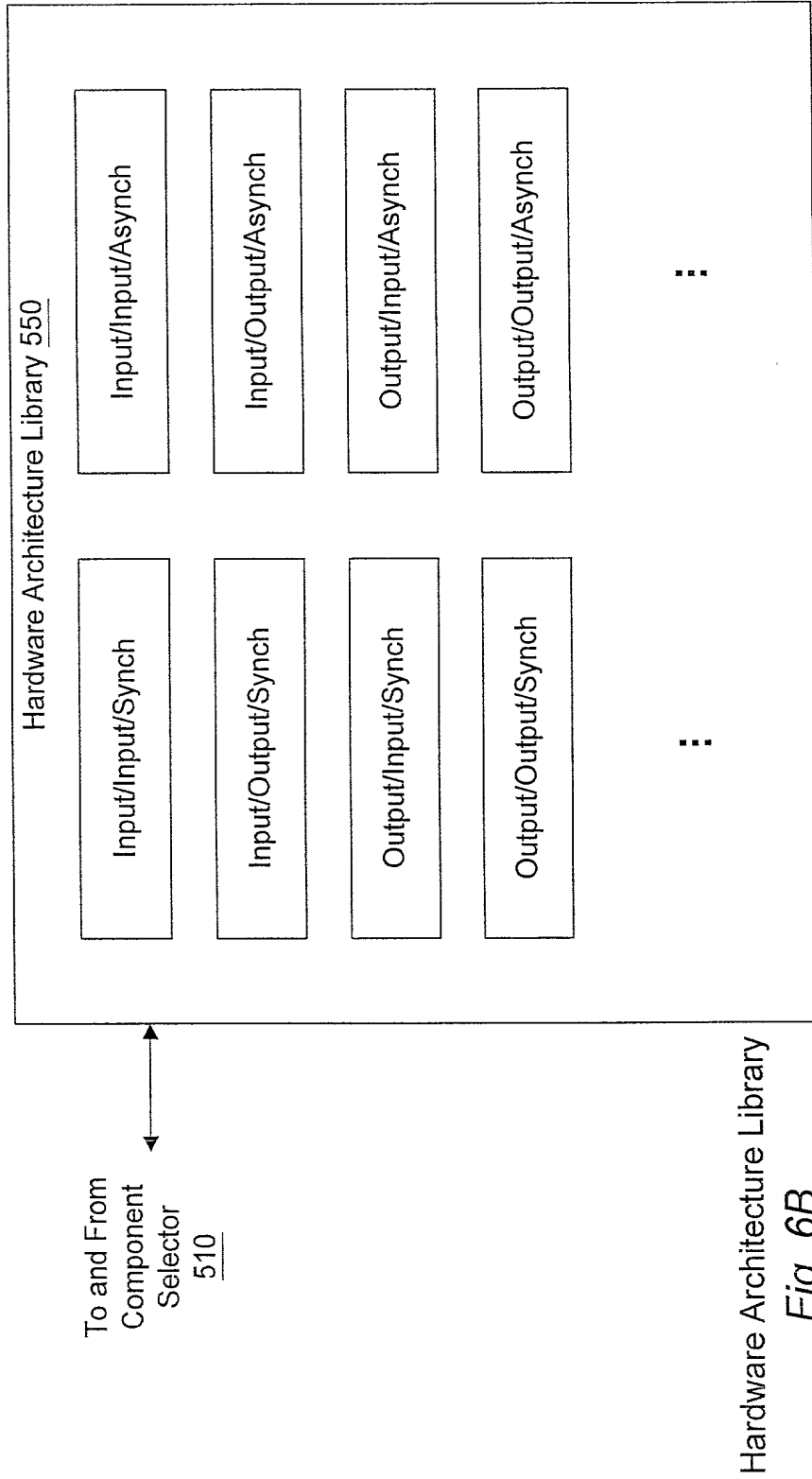


Fig. 6A





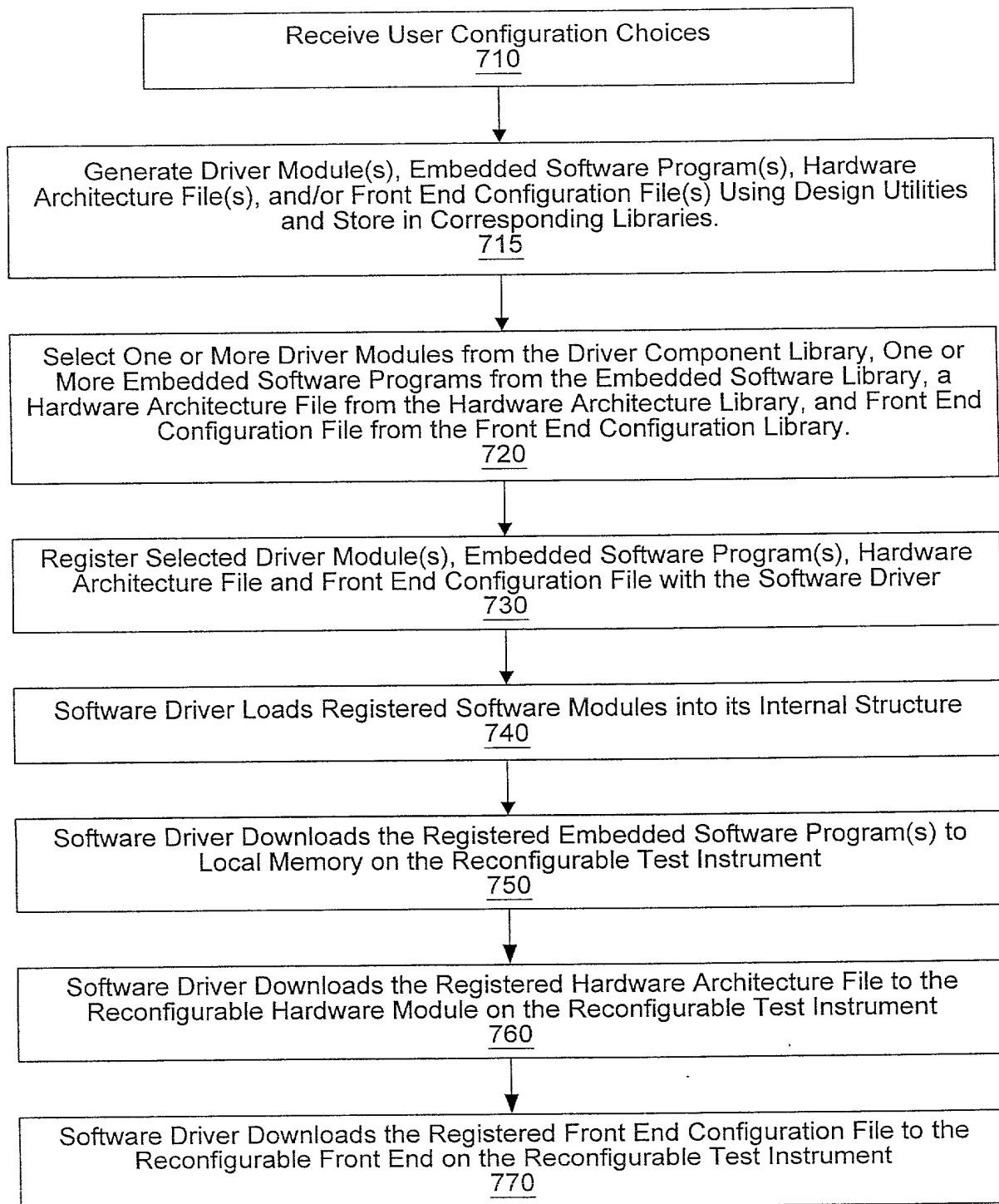
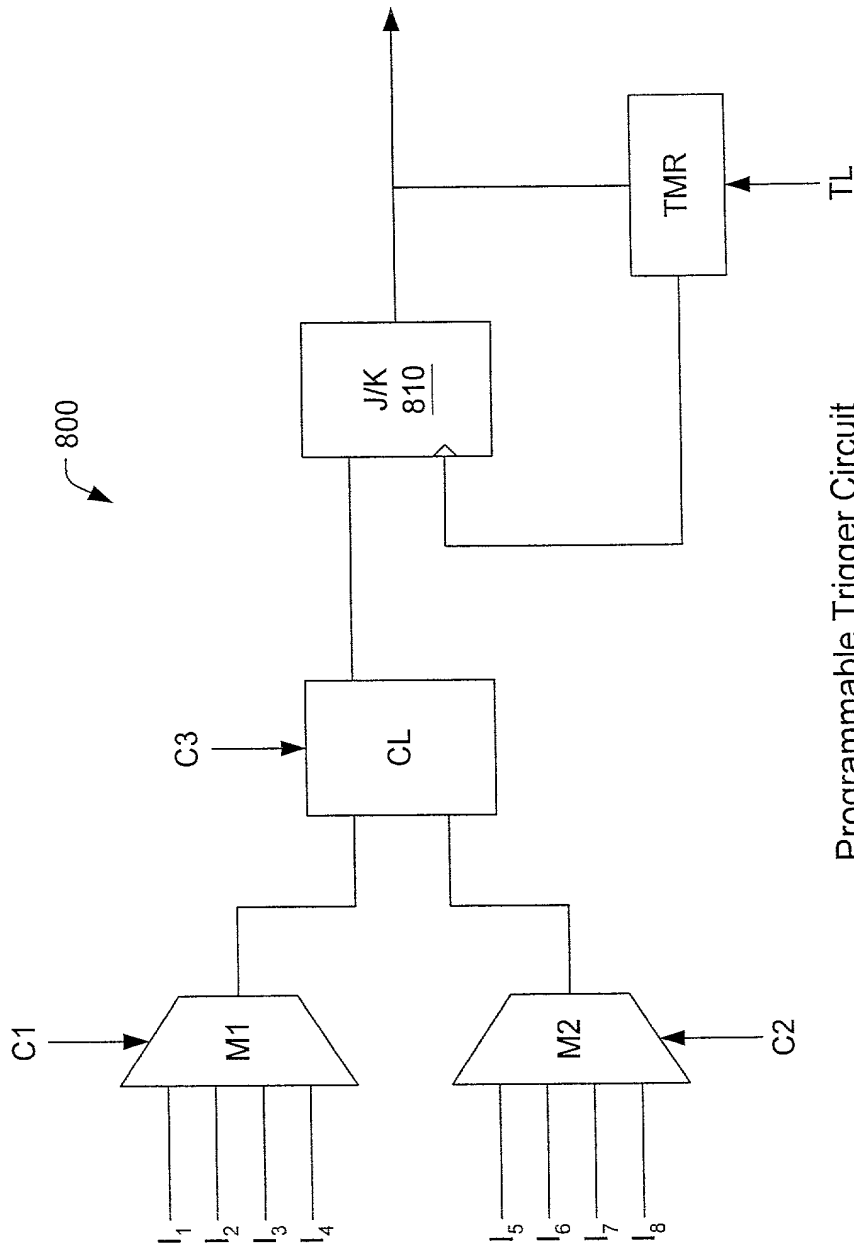


Fig. 7



Programmable Trigger Circuit  
Fig. 8